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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,287	01/23/2002	Burnell G. West	M-12401 US	9790

7590 11/29/2004

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EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,287	WEST, BURNELL G.	
	Examiner	Art Unit	
	John H Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19,26-32 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,26-32 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This office action is in response to applicant's amendment received on 11/03/2004.

Claims 1, 6-8, 10-19, 26, and 32 have been amended.

Claims 20-25, 33-42 have been cancelled.

Claim 43 has been added.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 10-14, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lloyd et al. (USP 6,434,211) in view of Loewenstein (USP 5,886,660).

Regarding claims 1 and 10, Lloyd et al. teach time stamping system (Abstract) comprising: an event stream distributor (pre-programmed sequence is implemented as software or hardware in a computer) coupled to receive the primary event stream, for apportioning events in the primary event stream across a plurality of secondary event stream (e.g. Fig.5, Col.3, lines 33-35, Col.6, lines 1-3, lines 24-40, Col.12, lines 37-63); and a plurality of timestamp circuits (e.g. Col.14, lines 3-14, Col.16, lines 27-28), each timestamp circuit coupled to receive a respective secondary event stream from the

event stream distributor (e.g. Col.10, lines 1-3, Col.16, lines 29-31), wherein each of the plurality of timestamp circuits record the times at which events occur in the respective received secondary event stream (e.g. Col.3, lines 15-25, Col.7, lines 11-27, lines 37-48), wherein each of the.

Regarding claims 2 and 11, Lloyd et al. teach an event rate in each of the secondary event streams is lower than an event rate in the primary event stream (Col.12, line 47-Col.13, line 5).

Regarding claims 3 and 12, Lloyd et al. teach the relative timing of the events in the primary event stream is maintained in each of the secondary event streams (Col.16, lines 1-19).

Regarding claims 4 and 13, Lloyd et al. teach the primary event stream is a differential signal (e.g. Fig.5, Col.12, 40-46).

Regarding claims 5 and 14, Lloyd et al. teach the secondary event streams are differential signals (e.g. Fig.5, Col.12, lines 47-63).

Regarding claim 43, Lloyd et al. teach the number of secondary event streams is a function of a maximum event rate in the primary event stream and a minimum period of elapse time between consecutive events for the timestamp circuit to accurately record all of the events in the primary event stream (e.g. Col.12, line 64-Col.13, lines 22).

Lloyd et al. teach fail to teach recorded times have a first component comprising a specific clock cycle of a reference clock and a second component comprising a time at which the given event occurs within the specific clock cycle.

Loewenstein teaches recorded times (time stamp) have a first component comprising a specific clock cycle of a reference clock (400) and a second component comprising a time at which the given event (402) occurs within the specific clock cycle (Fig.4, Col.5, lines 16-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include recorded times (time stamp) have a first component comprising a specific clock cycle of a reference clock (400) and a second component comprising a time at which the given event (402) occurs within the specific clock cycle as taught by Loewenstein in a timestamp system of Lloyd et al. for the purpose of providing advantageously measures the time at which an event occurs using one ramp signal and one analog-to-digital converter (ADC)(Loewenstein, Col.2, lines 19-20).

4. Claims 6-9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lloyd et al. (USP 6,434,211) in view of Loewenstein (USP 5,886,660) as applied to claims 1 and 10 above, and further in view of Boerker (US 2003/0035502 A1).

Regarding claims 6 and 7, Lloyd et al. and Loewenstein fail to teach distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate for generating a first one of the plurality of the secondary event streams, a second event in the primary event stream passes through a second gate for generating a second one of the plurality of the secondary event streams, and so on until an Nth event in the primary event stream

passes through an Nth gate for ;generating an Nth one of the plurality of the secondary event streams, wherein N is a positive integer.

Boerker teaches distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate for generating a first one of the plurality of the secondary event streams, a second event in the primary event stream passes through a second gate for generating a second one of the plurality of the secondary event streams, and so on until an Nth event in the primary event stream passes through an Nth gate for ,generating an Nth one of the plurality of the secondary event streams, wherein N is a positive integer ([0056], [0060], [0066], Fig.1, Fig.2).

Regarding claim 8, Boerker teaches apportioning rising edge events in the primary event stream among a set of the plurality of secondary event streams; and apportioning falling edge events in the primary event stream among a second set of plurality of secondary event streams ([0057]).

Regarding claims 9 and 19, Boerker teaches registering the events in each of the secondary event streams ([0055]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include step of distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream as taught by Boerker in a timestamp system of Lloyd et al. in view of Loewenstein for the purpose of providing an increasing transfer rate, data or

information is transferred via a transfer channel in shorter and shorter times (Boerker, [0005]).

5. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lloyd et al. (USP 6,434,211) in view of Loewenstein (USP 5,886,660) as applied to claim10 above, and further in view of Fransson (USP 5,940,467).

Regarding claims 15-18, Lloyd et al. and Loewenstein fail to teach a first counter coupled to receive the primary event stream; and a first plurality of gates coupled to the first counter, wherein the first counter is a Johnson counter, wherein the first counter is an N-bit counter, a second counter coupled to receive the primary event stream; and a second plurality of gates coupled to the second counter, a plurality of registers, each register operable to register events of one or more secondary event streams.

Fransson teaches a first counter 31 coupled to receive the primary event stream; and a first plurality of gates 71, 72, 73, 74, 75, 76 coupled to the first counter (Fig.1, Fig.2, Fig.3A), wherein the first counter is a Johnson counter, wherein the first counter is an N-bit counter (Col.2, lines 5-7), second counters 50-1, 50-2, 50-3, 50-4 coupled to receive the primary event stream (Fig.2); and a second plurality of gates of registers 99-1, 99-2, 99-3, 99-4 coupled to the second counter, each register operable to register events of one or more secondary event streams (Fig.8, Col.12, lines 45-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a counter, plurality of gates coupled to the counter, wherein the counter is a Johnson counter, wherein the counter is an N-bit counter as taught by Fransson in a timestamp system of Lloyd et al. in view of Loewenstein for the

purpose of providing a counting circuit, the resolution of which is equal to the cycle time of the first clock signal applied to the counting circuit (Fransson, Col.2, lines 46-48).

6. Claims 26-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fransson (USP 5,940,467) in view of Tambe et al. (USP 4,996,474).

Regarding claims 26-29, Fransson teaches a counting circuit, the circuit comprising: a first counter 31 coupled to receive the signal (Fig.1); and a first plurality of gates 71, 72, 73, 74, 75, 76, each gate of the first plurality of gates coupled to receive a signal and each gate of the first plurality of gates coupled to receive a respective control signal from the first counter 31 (Fig.2, Fig.5A), wherein the first plurality of gates are AND gates, wherein the signal is a differential signal, wherein the signal is a single-ended signal (Col.4, lines 39-65, Col.7, lines 32-67).

Regarding claim 30, Fransson teaches the counter is a Johnson counter (Col.2, lines 5-7).

Regarding claim 31, Fransson teaches the counter is an N-bit counter (Col.2, lines 5-7, Col.4, lines 14-19, Col.5, lines 43-45).

Regarding claim 32, Fransson teaches a second counter 50-1, 50-2, 50-3, 50-4 coupled to receive the primary event stream (Fig.2); and a second plurality of gates of registers 99-1, 99-2, 99-3, 99-4, each gate of the second plurality of gates coupled to receive the signal and each gate of the second plurality of gates coupled to receive a respective control signal from the second counter (Fig.8, Col.12, lines 45-65).

Fransson fails to teach the first counter coupled to receive the signal having a plurality of events and wherein the events of the signal are apportioned among the

outputs of the first plurality of gates as a function of the respective control signal from the first counter.

Tambe et al. teach the first counter (301) coupled to receive the signal (308) having a plurality of events (Col.3, lines 33-45, Col.4, lines 38-56) and wherein the events of the signal are apportioned among the outputs of the first plurality of gates as a function of the respective control signal from the first counter (Col.3, lines 33-45, Col.6, lines 58-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to inform the first counter coupled to receive the signal having a plurality of events and wherein the events of the signal are apportioned among the outputs of the first plurality of gates as a function of the respective control signal from the first counter as taught by Tambe et al. in a counting circuit of Fransson for the purpose of providing a method of digitally controlling the gate for a timing counter, to open and close the gate based on the occurrence of signal events (Tambe et al., Col.2, lines 22-25).

Response to Arguments

7. Applicant's arguments filed 11/03/2004 have been fully considered but they are not persuasive.

-Applicant argues that the prior did not teach "an event stream distributor coupled to receive the primary event stream, for apportioning events in the primary event stream across a plurality of secondary event stream" as cited in amended claims 1 and 10.

Lloyd et al. teach an event stream distributor (pre-programmed sequence is implemented as software or hardware in a computer) coupled to receive the primary event stream, for apportioning events in the primary event stream across a plurality of secondary event stream (e.g. Fig.5, Col.3, lines 33-35, Col.6, lines 1-3, lines 24-40, Col.12, lines 37-63).

-Applicant argues that the prior did not teach "the events of the signal are apportioned among the outputs of the first plurality of gates as a function of the respective control signal from the first counter" as cited in amended claim 26.

Tambe et al. teach the first counter (301) coupled to receive the signal (308) having a plurality of events (Col.3, lines 33-45, Col.4, lines 38-56) and wherein the events of the signal are apportioned among the outputs of the first plurality of gates as a function of the respective control signal from the first counter (Col.3, lines 33-45, Col.6, lines 58-63).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Specifically Lloyd et al., Loewenstein, and Tambe et al. have been added to another ground of rejection.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

November 20, 2004

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